

Docket No.: 247558US2RD/jkl

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

IN RE APPLICATION OF: Kensaku YAMAGUCHI, et al.

SERIAL NUMBER: 10/754,571

GROUP: 2439

FILED: January 12, 2004

EXAMINER: TURCHEN, JAMES R.

FOR: DATA ACCESS CONTROL METHOD FOR TAMPER RESISTANT  
MICROPROCESSOR USING CACHE MEMORY

**COMMENTS ON STATEMENT OF REASONS FOR ALLOWANCE**

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SIR:

Applicants acknowledge with appreciation the indication of Allowability of the claimed invention. In response to the Examiner's Statement of Reasons for Allowance in the Notice of Allowance of June 2, 2009, Applicants respectfully submit the following comments.

In the Examiner's Statement of Reasons for Allowance on page 4 of the Notice of Allowance mailed June 2, 2009, the paragraph starting on line 5 states in part:


The following is an examiner's statement of reasons for allowance: Examiner is unable to find prior art or any obvious combination thereof that discloses a cache memory configured to store the execution or data decrypted by the decryption unit and an actual encryption key used in decrypting the execution code or data for at least one cache line, the actual encryption key being stored in a secret protection attribute holding section of at least one cache line, the execution code or data stored in the cache memory remaining even after each program terminates.

Although the above comment seems to be directed to independent Claim 1, it is respectfully submitted that independent Claim 5 does not include all of the elements recited above. For example, Claim 5 recites a method comprising "reading" and "decrypting the execution code or data" and not a "decryption unit." Accordingly, it is respectfully submitted

that the above quoted statement applies only to independent Claim 1 (and claims dependent therefrom), and not to independent Claim 5 (and claims dependent therefrom), to the extent the language used in the statement differs from the language of the claims.

Respectfully Submitted,

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